Digital Integrated Circuits - 3663
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Team Gouda
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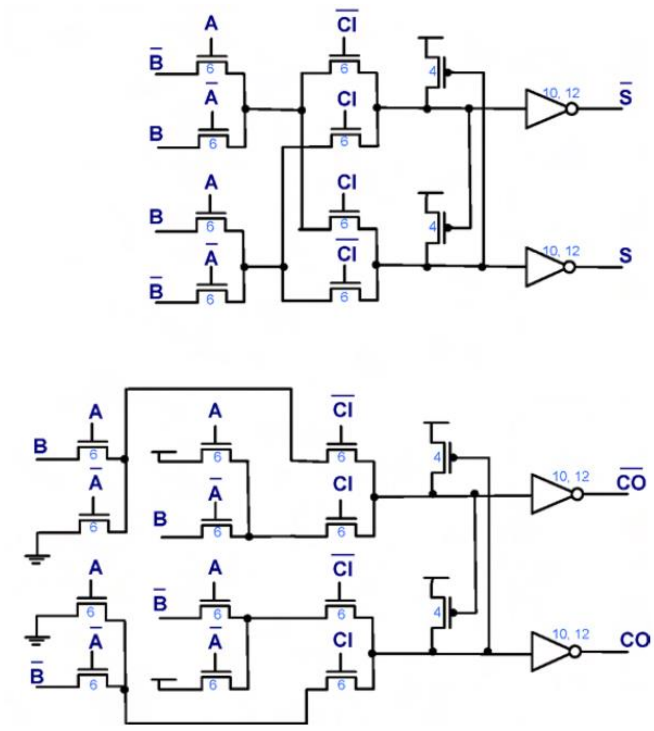
Design Project: Phase II
Due: 04/19/13, 12:00pm

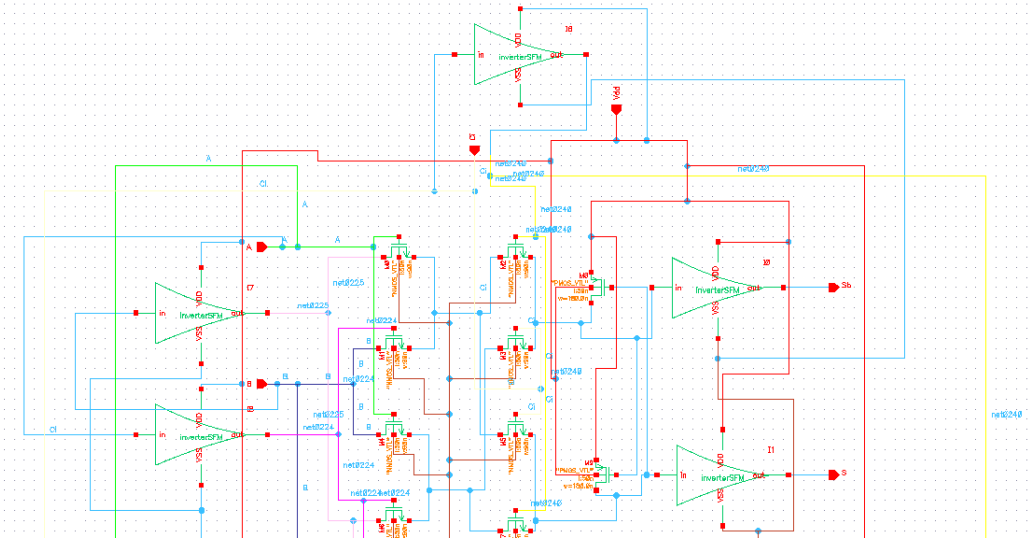
I. Schematics

i) Adder

a. The chosen adder was a Complementary Pass Transistor Logic (CPL) Full Adder, based off a design by Lixin Gao. The transistor schematic is as follows:

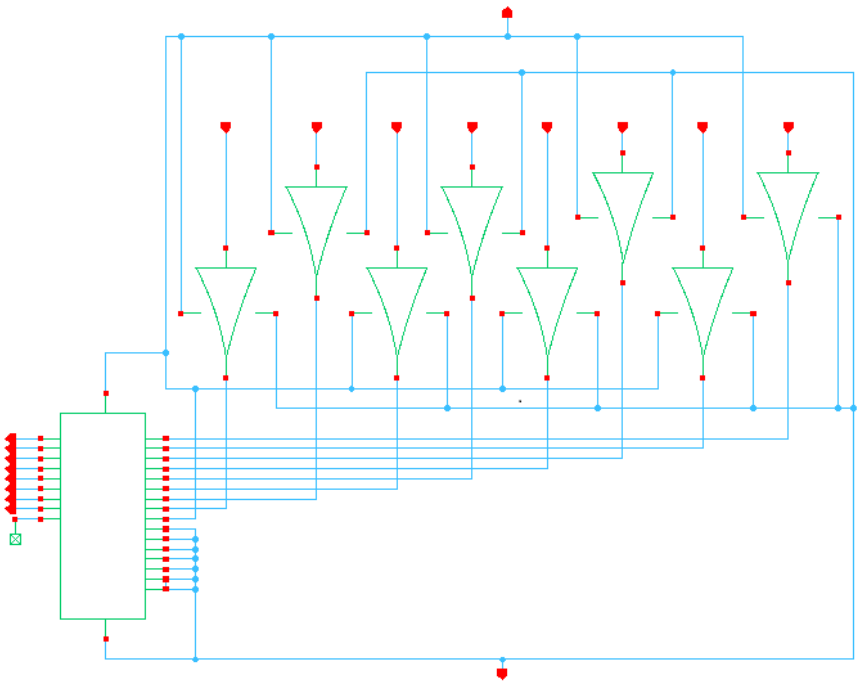


The useful ness of PTL is that, in some instances, there is a large gate count reduction, when compared to traditional CMOS layouts. One drawback is a “weak one” that is often encountered from NMOS transistors. To overcome this, CPL is used. After design in Cadence, the circuit was rather large. Depicted below is the top half of the CPL circuit.



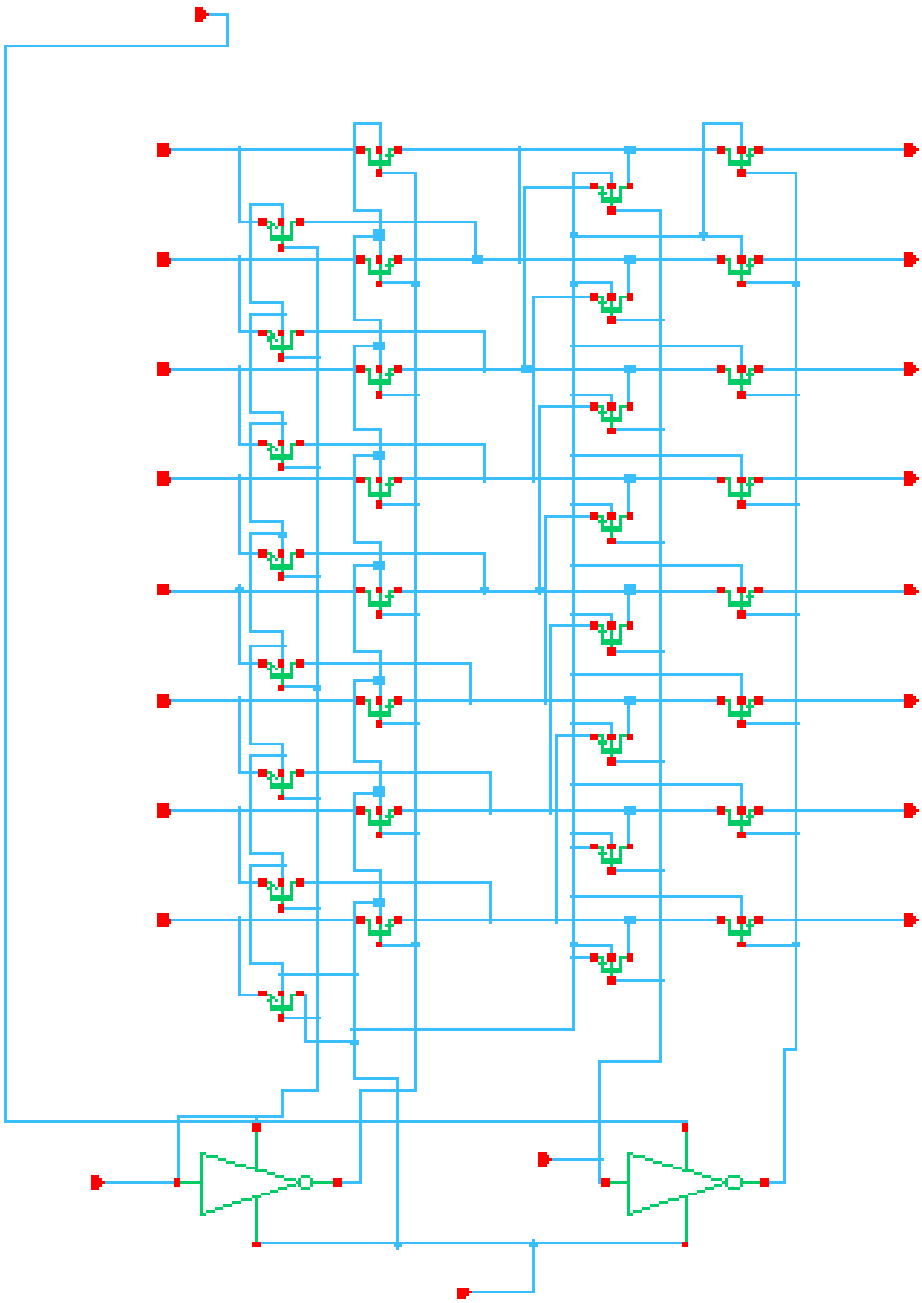
ii) TWOS COMP

a. Twos compliment was designed by running 8 bits of input data through inverters, and then adding 1 bit, which was done by utilizing the previously designed Full Adder. In the schematic below, the full adder is the block on the right, the inverters are on the top, and the output is on the left. On the adder, all bits, save the bit previously mentioned, were tied to ground.



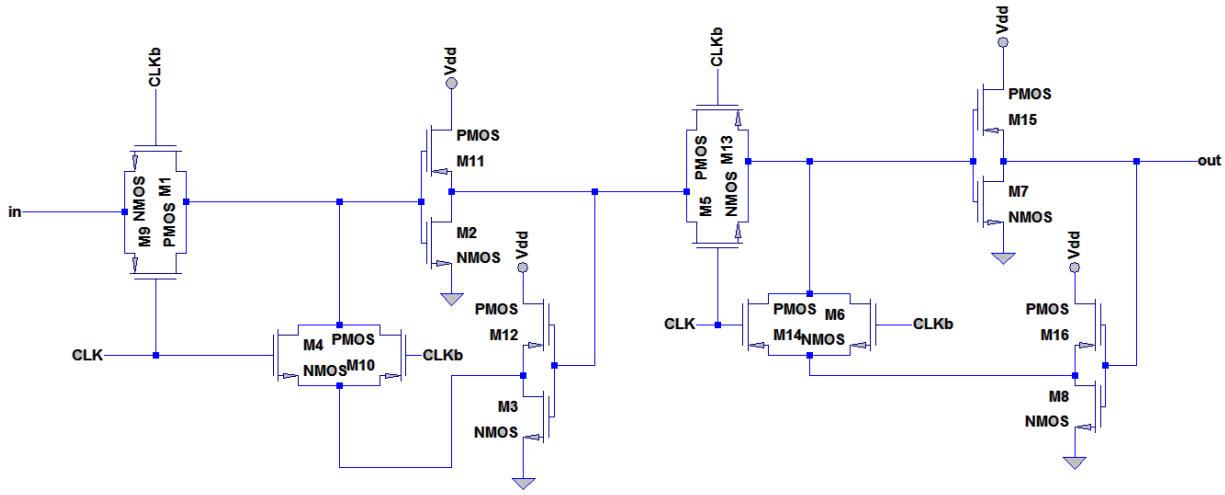
iii) SHIFT

a. The shifter borrows from the Rabaey text (p. 597), though in the implemented case we're working to shift left instead of right. The varied number of shifts is currently giving some trouble in the simulation, but with a little re-tooling, it should be handled very easily.



iv) 8BIT REG

a. This design was largely based off the schematic studied in class, mainly utilizing transmission gate logic.

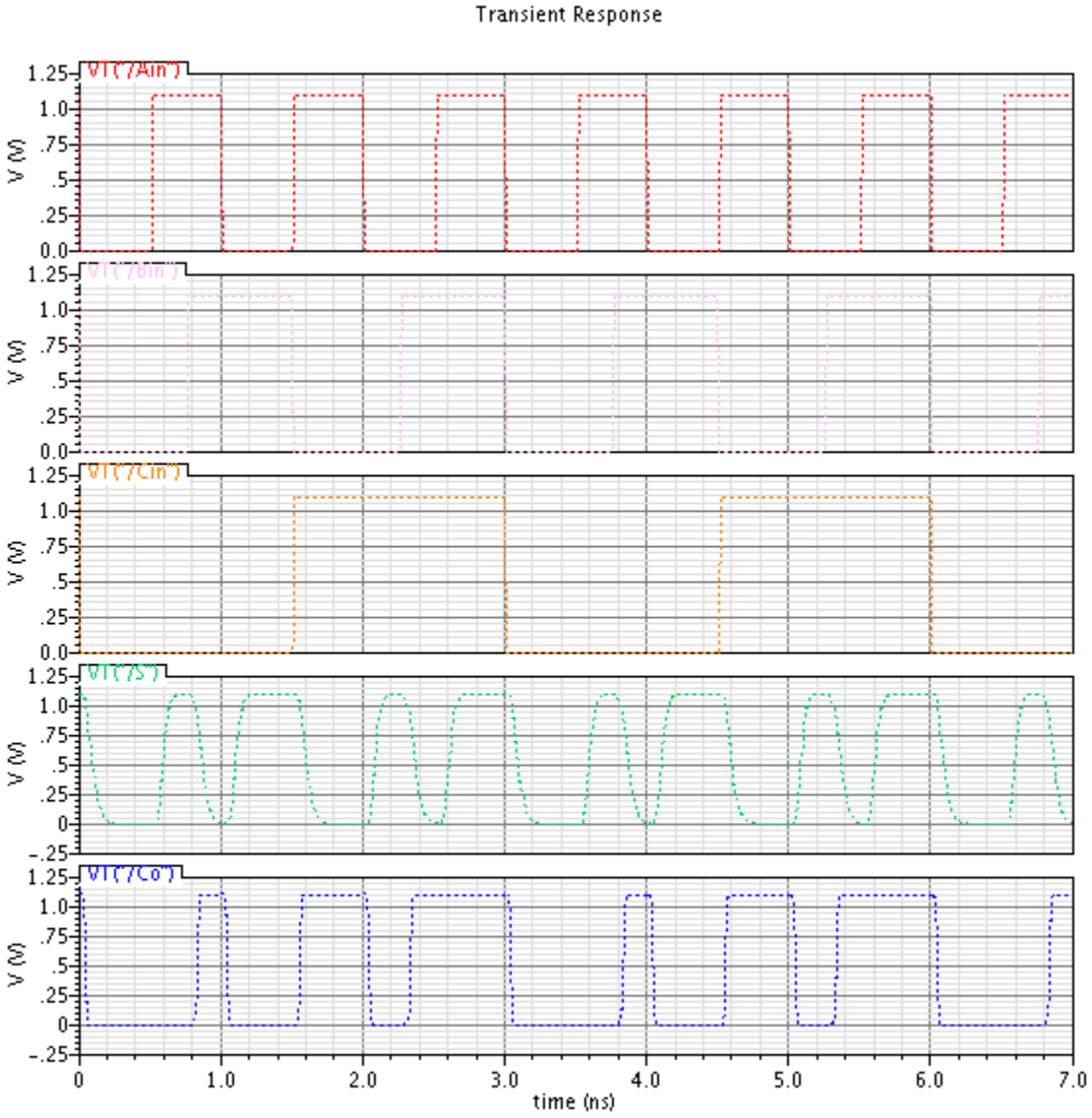


v) ALU

II. Simulations

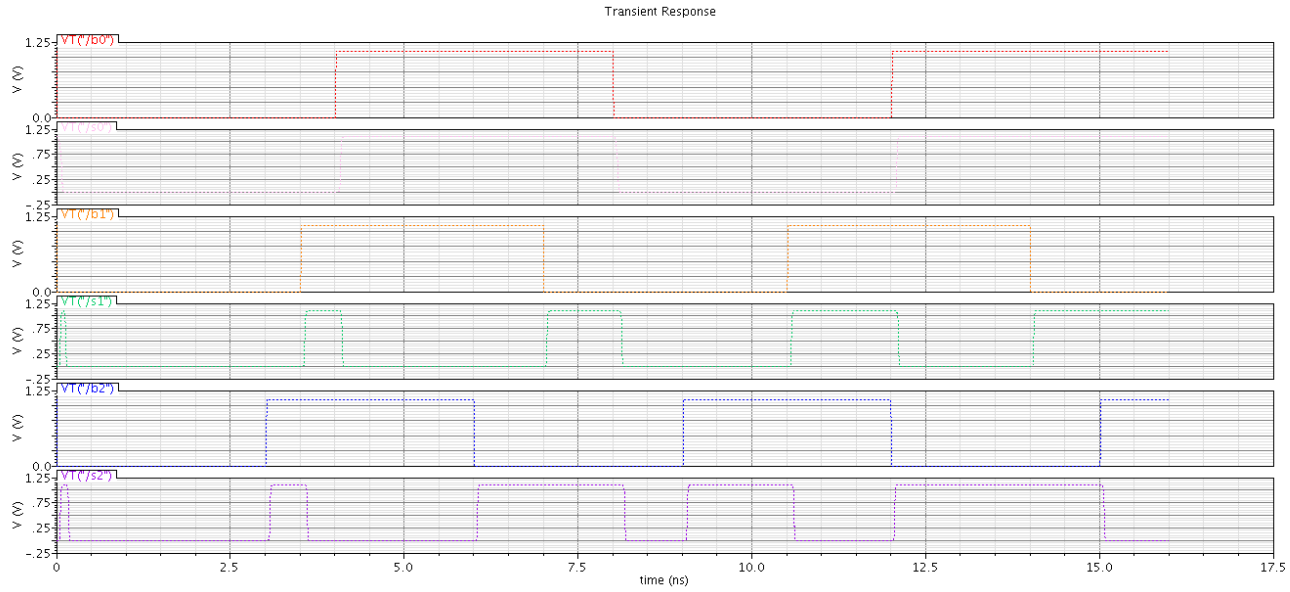
i) ADDER

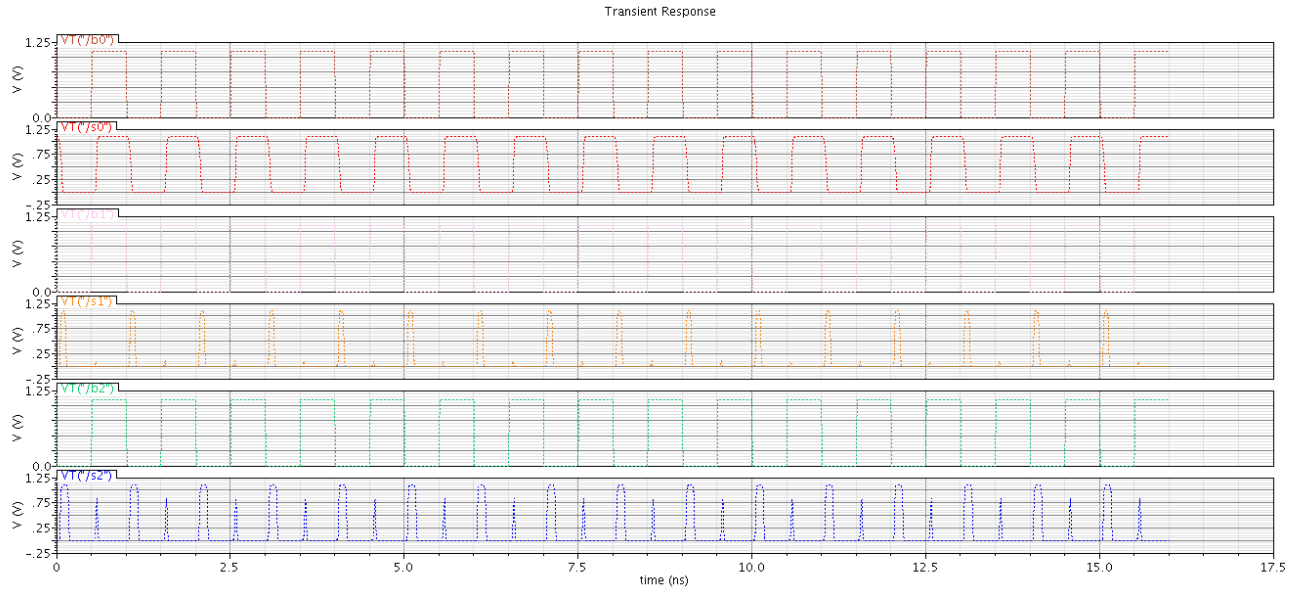
The following graph shows all possible inputs sweeping through the Adder, being variations across (A, B and Ci), with accompanying outputs (S and Co). To accomplish this in one simulation, the widths of the pulses was differentiated across the different inputs.



ii) TWOS COMP

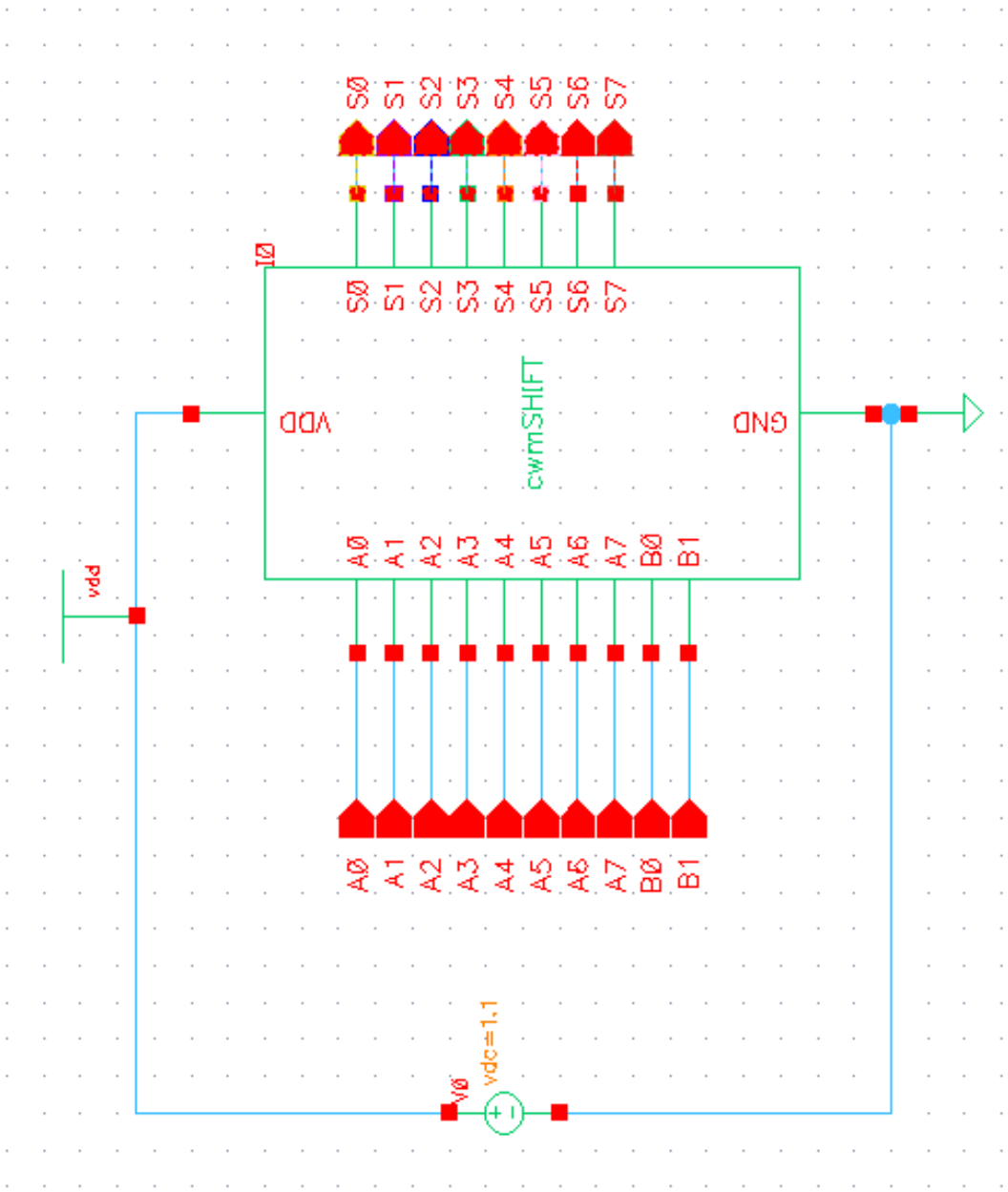
The first graph shows a simple modulation of inputs, while the second graph shows the outputs if all the inputs were set to one.

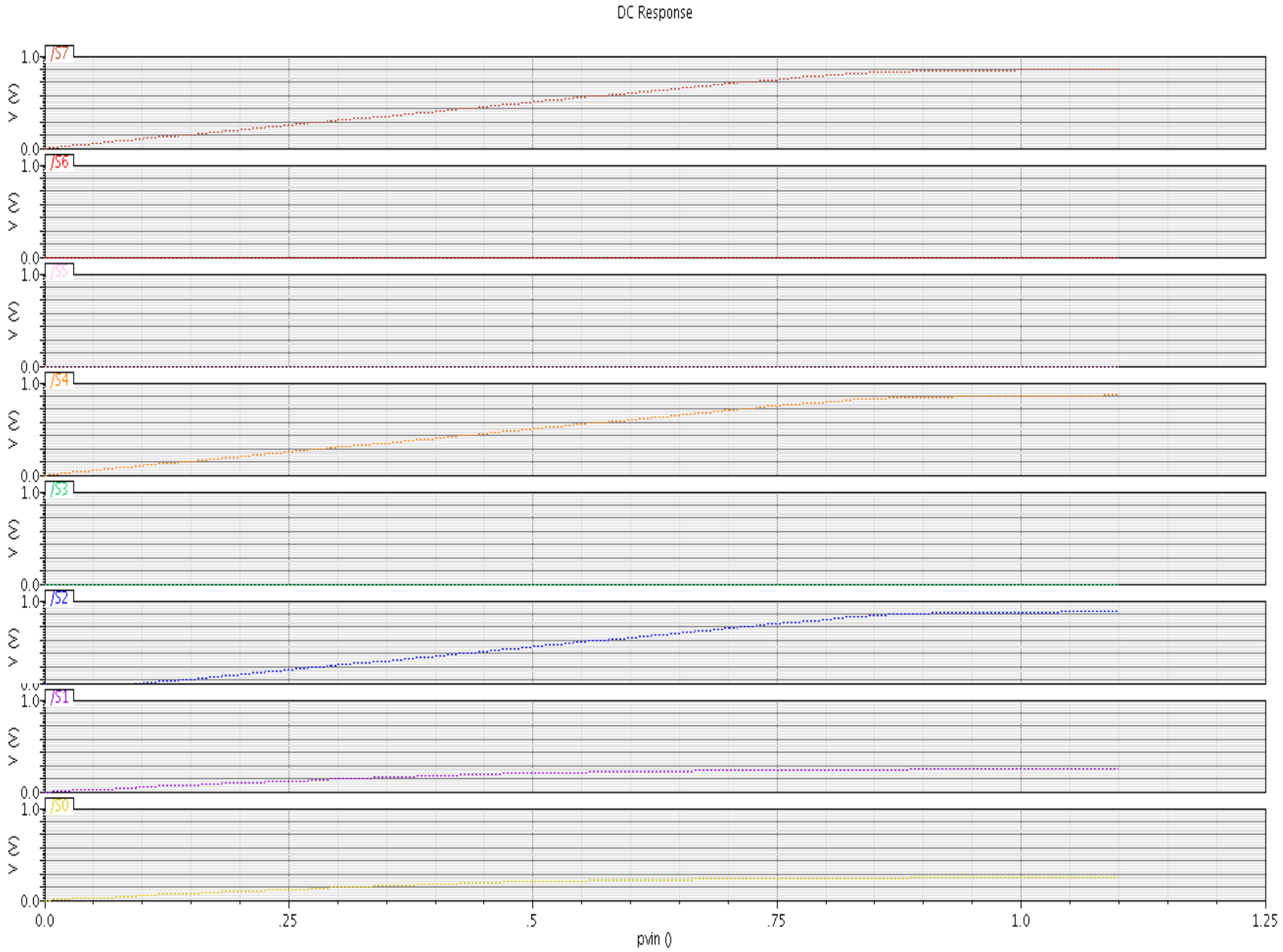

Transient Response
VT("/b0")
VT("/s0")
VT("/b1")
VT("/s1")
VT("/b2")
VT("/s2")
V (V)
1.25
.75
.25
-.25
0.0
0
2.5
5.0
7.5
10.0
12.5
15.0
17.5
time (ns)


Transient Response
VT("/b0")
VT("/s0")
VT("/b1")
VT("/s1")
VT("/b2")
VT("/s2")
V (V)
1.25
.75
.25
-.25
0.0
0
2.5
5.0
7.5
10.0
12.5
15.0
17.5
time (ns)

iii) SHIFT

The circuit requires a bit more re-tooling in Cadence to become fully operational. Graphs for a demonstrated set of inputs and a general test bench schematic are shown below.

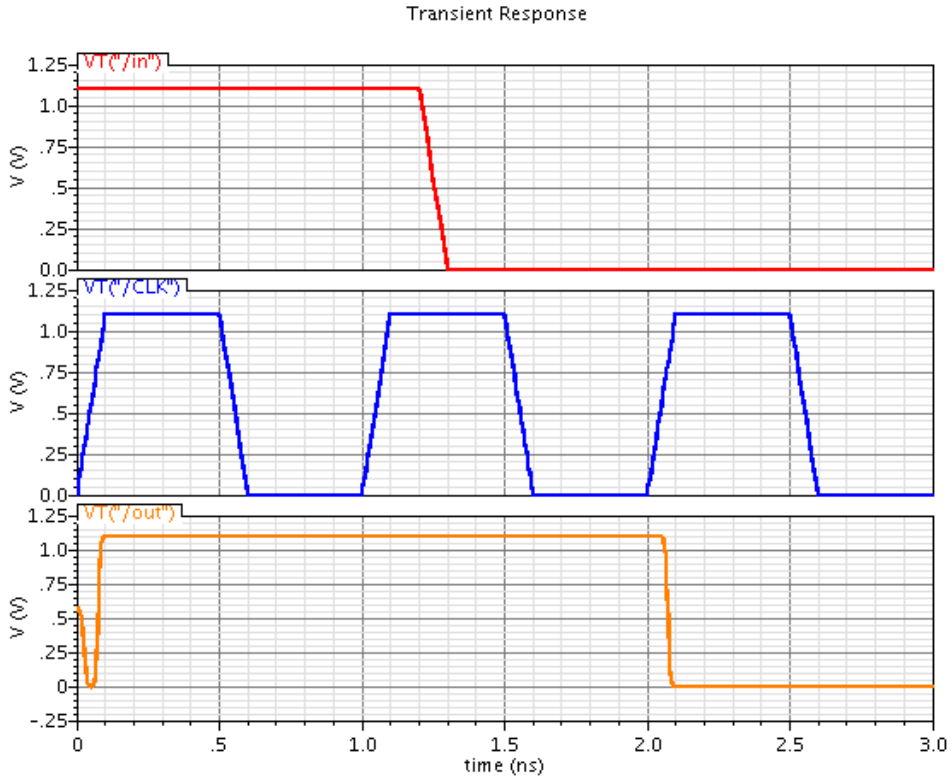


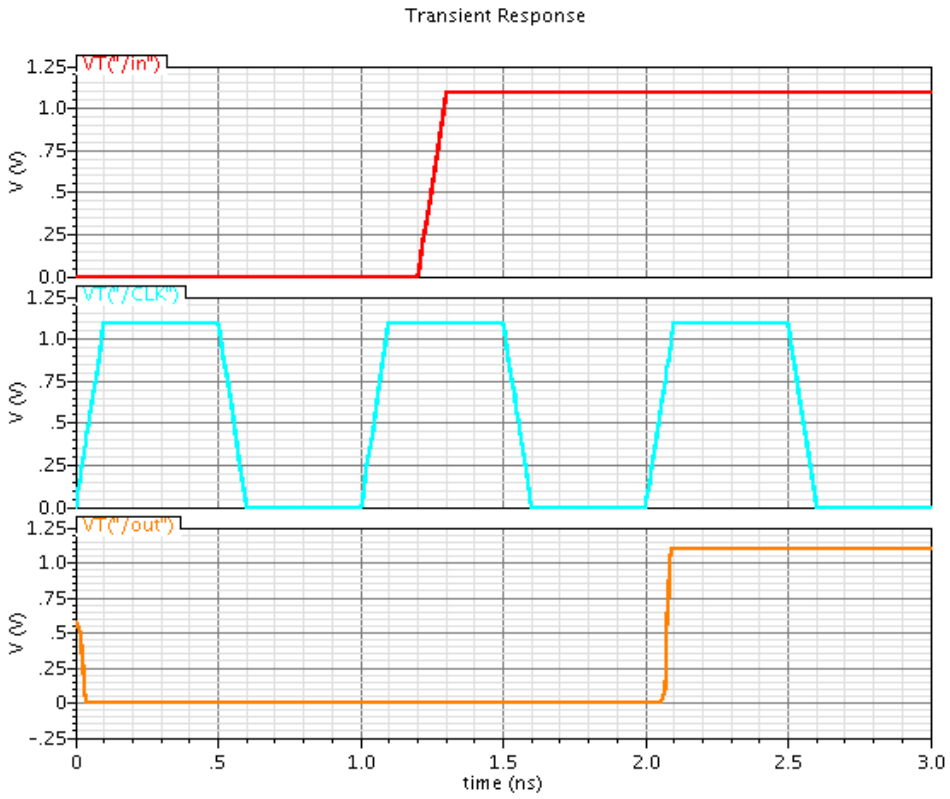


Single Shift. Input of 1100 1010

iv) 8BIT REG

The first graph shows the register input sweeping from high to low, and how the output reacts to that change. Dually, the second graph shows the input sweeping from low to high, and, again, how the output reacts.




Transient Response
VT("/in")
VT("/CLK")
VT("/out")
V (V)
1.25
1.0
.75
.5
.25
0.0
0
-.25
0
.5
1.0
1.5
2.0
2.5
3.0
time (ns)

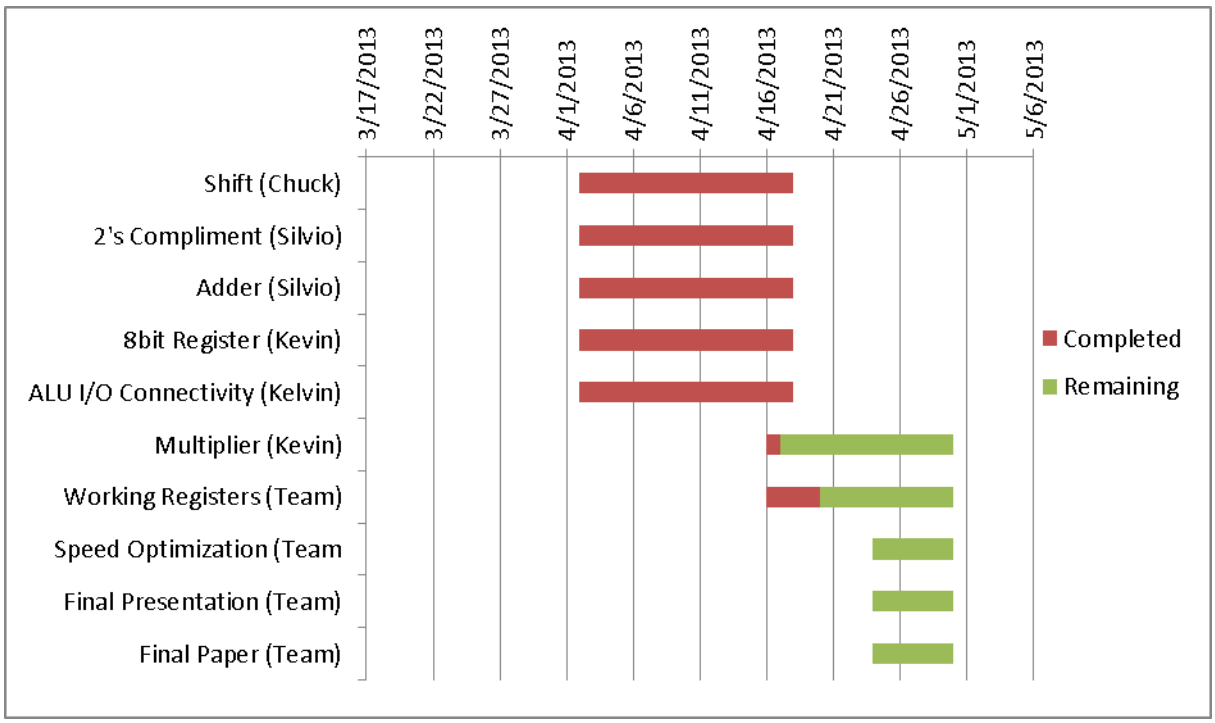
v) ALU

III. Progress Report

During this design phase, every member seemed to have asked themselves, at least once, “Do I actually know anything about anything regarding to Digital IC?” Eventually, every member found that the answer was a “yes.” The beginning of the second design phase started out with some turbulence, as everyone was not quite sure how to start; it’s safe to say that each member spent several days perusing through various design layouts, mostly through http://ieeexplore.ieee.org/, to ensure that the most appropriate design was selected. Each member chose a design that was not outside their respective scope of understanding and that fit the overall theme of the design.

The special function was finally finalized. Initially, it was going to be an encoder/decoder, but, after some review and consultation with the head designer, it was decided that the complexity would put the project slightly outside the budgeted time and fiscal allotment. To replace the encoder/decoder, the team has chosen to move forwards with designing a four-bit multiplier. The multiplier will be based around two components: the adder and the shifter, both of which, at this point in the design phase, are fully operational.

Team Gouda is still on track to finish at the designated time. To ensure this, along with the previously supplied simulation results, is a WBS, in the form of a Gantt chart:



IV. Delay Table

Operation	**Worst-Case Delay**	**Scenario**
ADD	39.95ps	tpLH (ABCi = 110 -» 111)
2COMP	48.48ps	tp(0000000-»1111111)
SHIFT	(**TBA)	[shift thrice]
AND	72.83ps	00->11
OR	76.87ps	00→01 or 10
Pass A	17.55ps	Passing 1 to 1